(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 324 619 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.07.2003 Bulletin 2003/27

(51) Int Cl.[7]: **H04N 7/62**, H04N 7/56, H03L 7/197, H04N 5/12

(21) Application number: **02022752.6**

(22) Date of filing: **11.10.2002**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **30.10.2001 IN DE10842001**

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(54) An improved fractional divider

(57) A method and an improved apparatus for clock recovery from data streams containing embedded reference clock values (29) **characterized in that** controlled clock source means consists of controllable digital Fractional Divider means (2.5) receiving a control value from digital comparator means (2.3) and a clock input from a digital clock synthesizer means (2.8) driven by a fixed oscillator means (2.7).

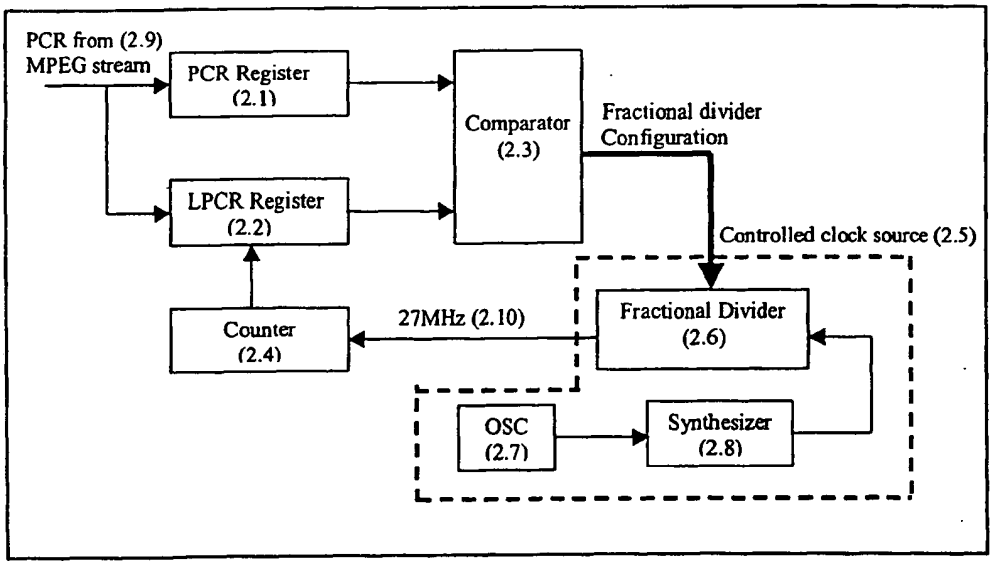

Figure 2

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Printed by Jouve, 75001 PARIS (FR)

REF. 2 DOCKET PU040057
CORRES. COUNTRY:
COUNTRY: PCT+US

Description

Field of the Invention

[0001] This invention relates to a method and an improved apparatus for clock recovery from data streams containing embedded reference clock values that uses purely digital techniques and can be incorporated without major changes in most existing applications such as MPEG based systems such as set-top boxes or DVD systems.

Background of the Invention

[0002] Many applications involving streaming data, such as streaming video contain embedded reference clock information to enable clock synchronization at the receiver. An important example of such data streams are Motion Picture Expert Group (MPEG) data streams that provide an efficient format for transmitting, receiving and storing video signals in digital format - the MPEG data stream format includes a timing reference fields called Program Clock Reference (PCR) or Elementary Stream Cock Reference (ESCR) that is embedded during the encoding process and serve to provide a clock synchronizing source. The PCR / ESCR field is extracted during the receive or playback process and is used to synchronize the receiving clock with the data stream rate thereby implementing clock recovery. The synchronizing or clock recovery function is implemented by a Digital Phase Locked Lop (DPLL).

[0003] Figure 1 shows a typical DPLL used in an MPEG receiver application. The MPEG encoding is performed using a reference 27MHz clock. To facilitate the clock recovery process at the decoder, the MPEG streams are periodically (typically every 0.1 sec) embedded with a timing reference field called Program Clock Reference (PCR). The PCR is generated as follows.

[0004] The 27 MHz system clock is given to a counter. A snapshot of the counter is taken periodically (rate at which the PCR has to be sent). The values of the counter thus obtained are stuffed into the PCR field of the MPEG stream.

[0005] On the decoding side the clock is recovered using the values in the PCR field.

[0006] The PCR in the MPEG stream is extracted and is stored in the received PCR register (1.1). The Local PCR register (1.2) stores the values of the PCR generated by the VCXO (1.6). By loading the contents of the counter (1.4) into local PCR register, when the MPEG stream with the PCR field updates the contents of received PCR register (1.1). The comparator (1.3) outputs an error signal depending on the difference between received PCR (1.1) and the local PCR (1.2). The error signal is used to drive a controlled clock source (1.7). Within the controlled clock source (1.7) the error signal is converted into analog voltage by the D/A converter (1.5). The analog output voltage from D/A converter (1.5) biases the VCXO (1.6) to generate the required frequency. The actual implementation may have some blocks being implemented in software. For example the compare function can be easily implemented in the software. The D/A block may consist of a PWM generator that is programmed by the software and a low pass filter.

[0007] US patent 5,473,385 describes a DPLL apparatus in which a subtractor gives the difference between received and Locally generated PCR values. The output of the subtractor, which is the error value is fed to a digital filter connected to the input of an accumulator. The accumulated error values are processed by an error signal generator, which produces a frequency adjustment signal for advancing or retarding the local oscillator frequency after gating with a selected video synchronization signal so that the clock frequency correction is performed only during the vertical synch or blanking interval and the effects of the synchronization are not visible. This technique does not permit easy modification of the characteristics of the PLL as there are no programmable features. Also, the dropping of clocks during the vertical synch incurs a significant risk in obtaining jitter-free reading of data. Finally, the implementation of this method requires major redesign of MPEG decoder circuits used in existing systems such as set-top boxes.

[0008] US patent 6,072,369 uses a phase error detector, interpolator, gain calculator, Digital to analog converter (DAC), voltage controlled oscillator (VCO) divider, Local PCR counter to generate the local clock signal. This scheme is implemented purely in hardware and uses analog components such as the DAC and VCO. It is therefore sensitive to noise and its characteristics are not easily modifiable.

[0009] US patent 6,175,385 describes three purely digital schemes that essentially use a fixed frequency oscillator. Clock synchronization is achieved by counting clock pulses of the fixed frequency signal and adjusting the unit for incrementing or decrementing the counted value to a predetermined value in a predetermined time according to the deviation of the fixed frequency from the reference frequency. The scheme requires a redesign of almost all the blocks used to process MPEG information in the majority of existing applications. Further, this process needs to be implemented during the video blanking interval and hence is limited to applications where such an interval is available.

The Summary of the Invention

[0010] The object of the invention is to obviate the above drawbacks by providing a completely digital implementation of the clock recovery systems.

[0011] The second object of the invention is to provide dynamically configurable loop filter characteristics.

[0012] Yet another object of the invention is to provide such an implementation where no major re design of the existing video information processing blocks is required.

[0013] To achieve the said objectives the present invention provides an improved apparatus for clock recovery from data streams containing embedded reference clock values comprising:

- Clock Reference storage means for storing clock reference values received from the incoming data stream connected to,
- input of a digital comparator means, the second input of which is connected to,
- Local Clock (LC) storage means for storing locally generated clock values provided by a,
- counter means which receives a clock signal from a controlled clock source means controlled by the output of said digital comparator means, **characterized in that**
- said controlled clock source means consists of a controllable digital Fractional Divider means receiving a control value from said digital comparator means and a clock input from a digital clock synthesizer means driven by a fixed oscillator means.

[0014] The said input data stream is an MPEG data stream in which said embedded clock reference value is either the Program Clock Reference (PCR) value or Elementary Stream Clock Reference (ESCR) value

[0015] The said comparator means is implemented using a microcontroller.

[0016] The said Digital Fractional Divider is any known Digital Fractional Divider.

[0017] The said Digital Fractional Divider is implemented as claimed in our co-pending application

[0018] The gain of said comparator means is adjusted in accordance with changing input conditions.

[0019] The gain of said comparator is adjusted to a high value prior to obtaining a match between said Local Clock and said Clock Reference and reduced after obtaining said match.

[0020] The present invention also provides a method for enabling clock recovery from data streams containing embedded reference clock values, comprising the steps of:

- storing the received reference clock values,
- generating a controlled local clock,
- comparing said received reference clock with said generated local clock;
- adjusting said controlled local clock to match said received reference clock;

characterized in that said controlled local clock is generated by performing controlled fractional division on the output from a fixed clock source.

[0021] The above method further includes adjusting of loop gain in accordance with changing input conditions.

[0022] The said loop gain is adjusted to a high value prior to lock-in and to a lower value after lock-in.

Brief Description of the drawings

[0023] The invention will now be described with reference to the accompanying drawings:

FIG. 1 shows a DPLL used in MPEG receiver application according to known art.

FIG. 2 shows the circuit diagram for the preferred embodiment of the invention.

FIG. 3 shows the fractional divider, described in our co-pending Indian patent application no. 1041/Del/2001 and its functioning in the instant invention.

Detailed Description

[0024] Figure 1 is described under the background of the invention.

[0025] Figure 2 shows the preferred embodiment of the invention. The PCR/ESCR from the data stream is extracted and stored in the PCR register (2.1). The LPCR register (2.2) stores the values of the PCR generated by the controlled clock source (2.5). On receiving a data stream with PCR/ESCR field, the PCR register (2.1) and LPCR register (2.2) are updated by loading into them the contents of PCR/ESCR field and the counter (2.4) respectively. The comparator (2.3) outputs the error signal depending upon the difference between PCR register (2.1) and LPCR register (2.2), which act as its inputs. The fractional divider (2.6) converts the error signal to the required frequency. The fractional divider (2.6) is clocked by a synthesizer (2.8), generating a high frequency clock (typically 600 MHz) with the help of reference frequency from a crystal oscillator (2.7).

[0026] The fractional divider (2.6) is responsible for the clock recovery scheme. The fractional divider could be any known fractional divider.

[0027] The preferred embodiment of the fractional divider is shown in figure 3 and is described in co-pending Indian patent application no. 1041/Del/2001.

[0028] The output from the synthesizer (2.8) of figure 2 is given to counter (3.1). The counter can be configured to divide by either n or n+1 depending upon the logic-state of the carry out. The fractional adder (3.2) is a binary adder. The fractional increment register (3.3) holds the fractional increment value. The contents of the fractional increment register are added to the current contents of fractional adder when clock enable is high and a rising synth clock edge.

[0029] By way of example, to get 27MHz clock the reference frequency of 600MHz from the synthesizer has to be divided by 22.222222. To achieve this, the counter (3.1) is programmed as divide by 22. The fractional increment value register is initialized with the fractional value viz., 0.222222. The counter (3.1) is such that when counter completes one programmed count, the clock out completes one clock cycle, simultaneously the contents of the fractional increment register (3.3) are added to the contents of fractional adder once every clock out

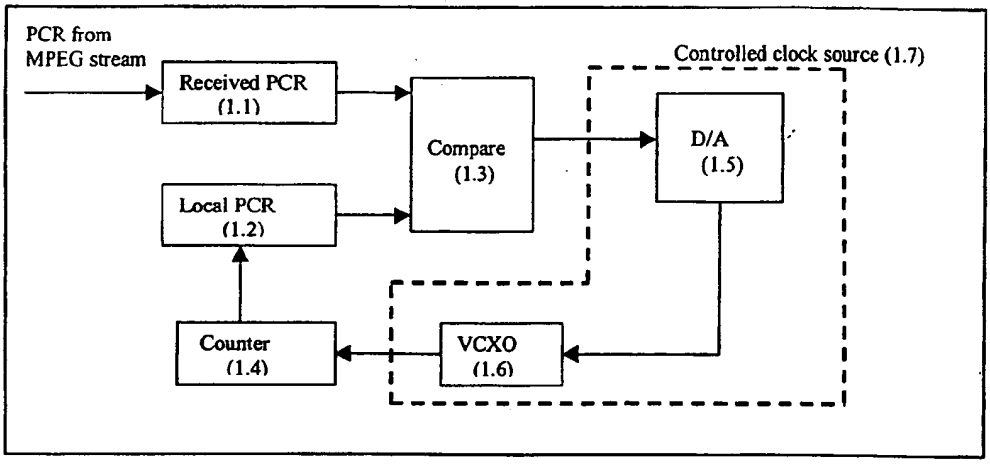
PCR from
MPEG stream
Received PCR
(1.1)
Local PCR
(1.2)
Compare
(1.3)
Counter
(1.4)
D/A
(1.5)
VCXO
(1.6)
Controlled clock source (1.7)

Figure 1

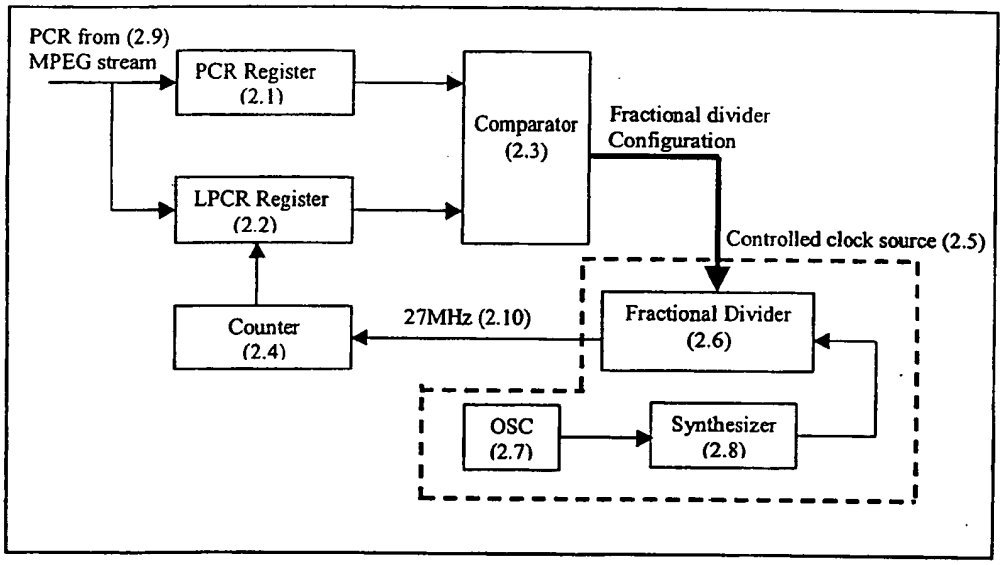
PCR from (2.9)
MPEG stream
PCR Register
(2.1)
LPCR Register
(2.2)
Comparator
(2.3)
Fractional divider
Configuration
Controlled clock source (2.5)
Counter
(2.4)
27MHz (2.10)
Fractional Divider
(2.6)
OSC
(2.7)
Synthesizer
(2.8)

Figure 2

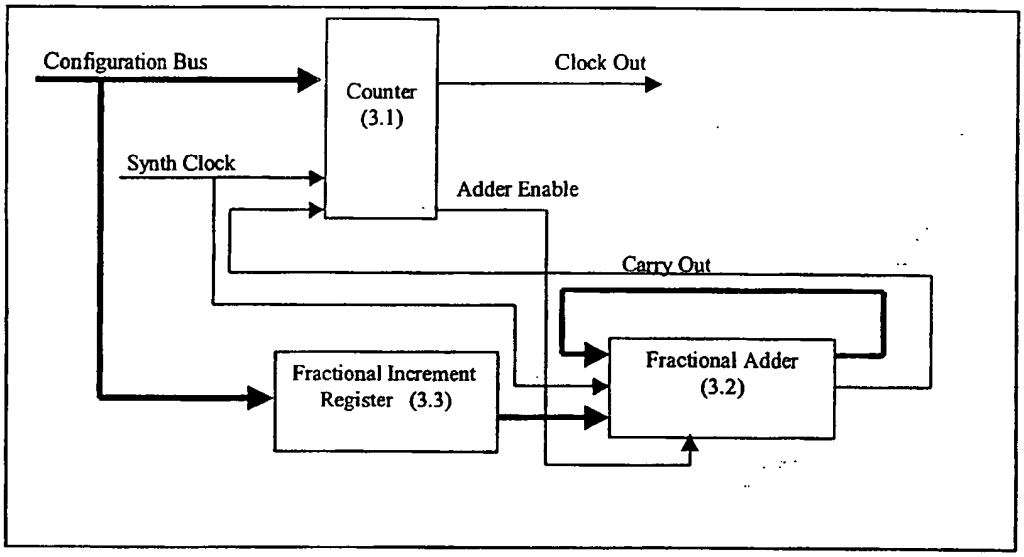
Configuration Bus
Counter
(3.1)
Clock Out
Synth Clock
Adder Enable
Carry Out
Fractional Increment
Register (3.3)
Fractional Adder
(3.2)

Figure 3

(19) Europäisches Patentamt
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(11) EP 1 324 619 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
13.08.2003 Bulletin 2003/33

(43) Date of publication A2:
02.07.2003 Bulletin 2003/27

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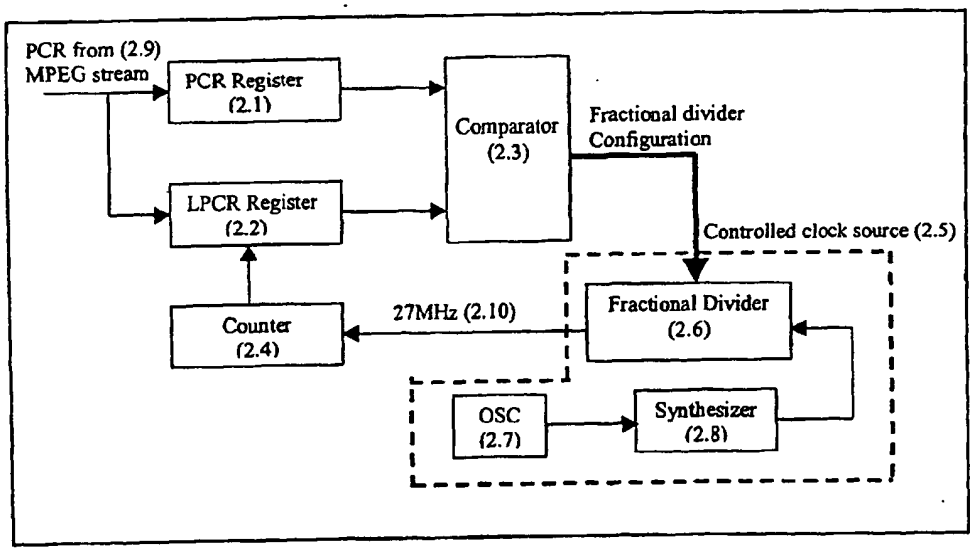

Figure 2

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EUROPEAN SEARCH REPORT

Application Number
EP 02 02 2752

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y,D	US 6 175 385 B1 (SHIRAI HIDEAKI ET AL) 16 January 2001 (2001-01-16)	1-5,8	H04N7/62 H04N7/56
A	* column 2, line 6 - line 37; figures 1-3 * * column 4, line 25 - column 11, line 8 * * column 18, line 16 - column 19, line 54 *	6,7,9,10	H03L7/197 H04N5/12 H03L7/00
Y	EP 0 413 473 A (DELCO ELECTRONICS CORP) 20 February 1991 (1991-02-20)	1-5,8	
A	* column 4, line 52 - column 6, line 38; figure 4 *	6,7,9,10	
Y	SATO F ET AL: "Digital phase-locked loop with wide lock-in range using fractional divider" COMMUNICATIONS, COMPUTERS AND SIGNAL PROCESSING, 1993., IEEE PACIFIC RIM CONFERENCE ON VICTORIA, BC, CANADA 19-21 MAY 1993, NEW YORK, NY, USA,IEEE, 19 May 1993 (1993-05-19), pages 431-434, XP010141765 ISBN: 0-7803-0971-5	1-5,8	
A	* page 431 - page 433, left-hand column, line 35; figure 1 *	6,7,9,10	
A,D	US 6 072 369 A (CHOI KWANG-HO ET AL) 6 June 2000 (2000-06-06) * column 5, line 39 - line 48; figure 2 *	1-12	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H04N
H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	24 June 2003	McGrath, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 02 2752

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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24-06-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EP 0413473 A	20-02-1991	US 4972446 A	20-11-1990
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82